WHAT IS CLAIMED IS:

1. An adaptive computing integrated circuit configurable to perform a plurality of functions, comprising:

a plurality of heterogeneous computational elements; and

an interconnection network coupled to the plurality of heterogeneous computational elements, the interconnection network operative to configure the plurality of heterogeneous computational elements;

wherein a first group of heterogeneous computational elements is configurable to form a first functional unit to implement a first function;

wherein a second group of heterogeneous computational elements is configurable to form a second functional unit to implement a second function; and

wherein if the second function is not currently used, one or more of the second group of heterogeneous computational elements are reconfigurable by the interconnection network to implement the first function.

2. The adaptive computing integrated circuit of claim 1 wherein if the second function is not currently used, the one or more of the second group of heterogeneous computational elements are reconfigurable to implement the first function by forming one or more additional instances of the first functional unit.

3. The adaptive computing integrated circuit of claim 1 wherein if the second function is not currently used, one or more of the first group of heterogeneous computational elements and the one or more of the second group of heterogeneous computational elements are reconfigurable to form a single functional unit to implement the first function.

4. The adaptive computing integrated circuit of claim 1 wherein if the second function is not currently used, the one or more of the second group of heterogeneous computational elements are reconfigurable by the interconnection network to implement one or more of the plurality of functions other than the second function.

5. The adaptive computing integrated circuit of claim 1 wherein if a third function is to be implemented, one or more of the first group of heterogeneous computational elements and/or the one or more of the second group of heterogeneous computational elements are reconfigurable by the interconnection network to implement the third function.

6. An adaptive computing integrated circuit, comprising:

a plurality of reconfigurable matrices, the plurality of reconfigurable matrices including a plurality of heterogeneous computational units, each heterogeneous computational unit having a plurality of fixed computational elements, the plurality of fixed computational elements including a first computational element having a first architecture and a second computational element having a second architecture, the first architecture distinct from the second architecture, the plurality of heterogeneous computational units coupled to an interconnect network and reconfigurable in response to configuration information; and

a matrix interconnection network coupled to the plurality of reconfigurable matrices, the matrix interconnection network operative to reconfigure the plurality of reconfigurable matrices in response to the configuration information for a plurality of operating modes;

wherein a first group of heterogeneous computational units is reconfigurable to form a first functional unit to implement a first operating mode;

wherein a second group of heterogeneous computational units is reconfigurable to form a second functional unit to implement a second operating mode;

wherein if the second operating mode is not currently used, one or more of the second group of heterogeneous computational units are reconfigurable to implement the first operating mode.

7. The adaptive computing integrated circuit of claim 6 wherein if the second operating mode is not currently used, the one or more of the second group of heterogeneous computational units are reconfigurable to implement the first operating mode by forming one or more additional instances of the first functional unit.

8. The adaptive computing integrated circuit of claim 6 wherein if the second operating mode is not currently used, one or more of the first group of heterogeneous computational units and the one or more of the second group of heterogeneous computational units are reconfigurable to form a single functional unit to implement the first operating mode.

9. The adaptive computing integrated circuit of claim 6 wherein if the second operating mode is not currently used, the one or more of the second group of

heterogeneous computational units are reconfigurable to implement one or more of the plurality of operating modes other than the second operating mode.

10. The adaptive computing integrated circuit of claim 6 wherein if a third operating mode is to be implemented, one or more of the first group of heterogeneous computational units and/or the one or more of the second group of heterogeneous computational units are reconfigurable to implement the third operating mode.

11. An adaptive computing integrated circuit, comprising:

a plurality of heterogeneous computational elements, the plurality of heterogeneous computational elements including a first computational element and a second computational element, the first computational element having a first fixed architecture of a plurality of fixed architecture and the second computational element having a second fixed architecture of the plurality of fixed architectures, the first fixed architecture being different than the second fixed architecture, and the plurality of fixed architectures including functions for memory, addition, multiplication, complex multiplication, subtraction, configuration, reconfiguration, control, input, output, and field programmability; and

an interconnection network coupled to the plurality of heterogeneous computational elements, the interconnection network operative to configure the plurality of heterogeneous computational elements;

wherein a first group of heterogeneous computational elements is reconfigurable to form a first functional unit to implement a first function;

wherein a second group of heterogeneous computational elements is reconfigurable to form a second functional unit to implement a second function; and

wherein if the second function is not currently used, one or more of the second group of heterogeneous computational elements are reconfigurable by the interconnection network to implement the first function.

12. The adaptive computing integrated circuit of claim 11 wherein if the second function is not currently used, the one or more of the second group of heterogeneous computational elements are reconfigurable to implement the first function by forming one or more additional instances of the first functional unit.

13. The adaptive computing integrated circuit of claim 11 wherein if the second function is not currently used, one or more of the first group of heterogeneous

computational elements and the one or more of the second group of heterogeneous computational elements are reconfigurable to form a single functional unit to implement the first function.

14. The adaptive computing integrated circuit of claim 11 wherein if the second function is not currently used, the one or more of the second group of heterogeneous computational elements are reconfigurable by the interconnection network to implement one or more of the plurality of functions other than the second function.

15. The adaptive computing integrated circuit of claim 11 wherein if a third function is to be implemented, one or more of the first group of heterogeneous computational elements and/or the one or more of the second group of heterogeneous computational elements are reconfigurable by the interconnection network to implement the third function.

16. An adaptive computing integrated circuit, comprising:

a plurality of heterogeneous computational elements, the plurality of heterogeneous computational elements including a first computational element and a second computational element, the first computational element having a first fixed architecture and the second computational element having a second fixed architecture, the first fixed architecture being different than the second fixed architecture; and

an interconnection network coupled to the plurality of heterogeneous computational elements, the interconnection network operative to configure a first group of heterogeneous computational elements to form a first functional unit for a first functional mode of a plurality of functional modes, in response to first configuration information, and the interconnection network further operative to reconfigure a second group of heterogeneous computational elements to form a second functional unit for a second functional mode of the plurality of functional modes, in response to second configuration information, the first functional mode being different than the second functional mode, and the plurality of functional modes including linear algorithmic operations, non-linear algorithmic operations, finite state machine operations, memory operations, and bit-level manipulations;

wherein if the second functional mode is not currently used, one or more of the second group of heterogeneous computational units are reconfigurable to implement the first functional mode.

17. The adaptive computing integrated circuit of claim 16 wherein if the second functional mode is not currently used, the one or more of the second group of heterogeneous computational elements are reconfigurable to implement the first functional mode by forming one or more additional instances of the first functional unit.

18. The adaptive computing integrated circuit of claim 16 wherein if the second functional mode is not currently used, one or more of the first group of heterogeneous computational elements and the one or more of the second group of heterogeneous computational elements are reconfigurable to form a single functional unit to implement the first functional mode.

19. The adaptive computing integrated circuit of claim 16 wherein if the second functional mode is not currently used, the one or more of the second group of heterogeneous computational elements are reconfigurable by the interconnection network to implement one or more of the plurality of functional modes other than the second functional mode.

20. The adaptive computing integrated circuit of claim 16 wherein if a third functional mode is to be implemented, one or more of the first group of heterogeneous computational elements and/or the one or more of the second group of heterogeneous computational elements are reconfigurable by the interconnection network to implement the third functional mode.

21. A method for allocating hardware resources within an adaptive computing integrated circuit, comprising:

in response to first configuration information, configuring a first group of heterogeneous computational elements to form a first functional unit to implement a first function and configuring a second group of heterogeneous computational elements to form a second functional unit to implement a second function; and

in response to second configuration information, reconfiguring one or more of the second group of heterogeneous computational elements to implement the first function.

22. The method of claim 21 wherein the second configuration information is generated when the second function is not currently used.

23. The method of claim 21 wherein in response to the second configuration information, the one or more of the second group of heterogeneous computational elements are reconfigured to form one or more additional instances of the first functional unit to implement the first function.

24. The method of claim 21 wherein in response to the second configuration information, one or more of the first group of heterogeneous computational elements and the one or more of the second group of heterogeneous computational elements are reconfigured to form a single functional unit to implement the first function.

25. The method of claim 21 further comprising:

in response to third configuration information, reconfiguring one or more of the first group of heterogeneous computational elements and/or the one or more of the second group of heterogeneous computational elements to implement a third function.